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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/587,080	07/21/2006	Hiroki Mouri	28951.1181	9532

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EXAMINER	
FISCHER, MARK L	
ART UNIT	PAPER NUMBER
2627	
MAIL DATE	DELIVERY MODE
10/09/2009	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/587,080	MOURI ET AL.	
	Examiner	Art Unit	
	Mark Fischer	2627	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 July 2009*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-4,9-12 and 20-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-4,9-12 and 20-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 July 2009* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

1. This Office Action is in response to the Amendment filed on July 1, 2009.

Drawings

2. A replacement drawing for Figure 5 was received on July 1, 2009. This drawing is acceptable and has been entered into the record.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out

the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 2, 3, 10-12, and 20-22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (hereinafter AAPA) in view of Tomimoto (JP 2000-243034).

Regarding claim 2, AAPA discloses a signal processing apparatus (Fig. 5) comprising: a variable gain amplifier (102) for automatically adjusting a signal read from a recording medium so that the signal has a desired amplitude; a filter circuit (103) for removing a signal in a specific band, said filter circuit being connected to the variable gain amplifier; an A/D converter (104) for converting an analog signal into a digital signal, said converter being connected to the filter circuit; an automatic gain controller (105) being connected to the A/D converter; a waveform equalizer (106) for performing waveform equalization, said equalizer being connected to the A/D converter; a control circuit (107) for performing baseline control for the output of the waveform equalizer and the output of the A/D converter (the output of the A/D converter 104 is present in the output of DEQ 106) on the basis of the output of the waveform equalizer; an adaptive transversal filter (108) for amplifying a signal in a specific band as well as performing waveform equalization for a reproduction signal, the A/D converter being baseline-controlled (output of 107 is fed back to 104); a detection circuit (110) for performing error detection and correction using a LMS (Least Mean Square) algorithm, said detection circuit being connected to the adaptive transversal filter; a decoder (109) for performing maximum likelihood decoding, said decoder being connected to the adaptive transversal filter; and a timing recovery logic circuit (111) for extracting a reproduction clock, said logic circuit being connected to the control circuit.

AAPA does not explicitly disclose that the adaptive transversal filter is connected to the output of the A/D converter. However, Tomimoto discloses (Fig. 1) the connection of a FIR filter (3) to the output of an A/D converter (1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA with Tomimoto with the motivation to stabilize the reading of a signal and prevent interference between the filter 108 of AAPA and the PLL circuit (106, 107, 111, 112, 113) of AAPA.

Regarding claim 3, AAPA discloses a signal processing apparatus (Fig. 5) comprising: a variable gain amplifier (102) for automatically adjusting a signal read from a recording medium so that the signal has a desired amplitude; an A/D converter (104) for converting an analog signal into a digital signal, said converter being connected to the variable gain amplifier; an automatic gain controller (105) being connected to the A/D converter; a waveform equalizer (106) for performing waveform equalization, said equalizer being connected to the A/D converter; a control circuit (107) for performing baseline control-for the output of the waveform equalizer and the output of the A/D converter (the output of the A/D converter 104 is present in the output of DEQ 106) on the basis of the output of the waveform equalizer; an adaptive transversal filter (108) for amplifying a signal in a specific band as well as performing waveform equalization for a reproduction signal, the A/D converter being baseline-controlled (output of 107 is fed back to 104); a detection circuit (110)for performing error detection and correction using a LMS (Least Mean Square) algorithm, said detection circuit being connected to the adaptive transversal filter; a decoder (109) for performing maximum likelihood decoding, said decoder being connected to the adaptive transversal filter; and a timing recovery logic circuit (111) for extracting a reproduction clock, said logic circuit being connected to the control circuit. AAPA does not

explicitly disclose that the adaptive transversal filter is connected to the output of the A/D converter. However, Tomimoto discloses (Fig. 1) the connection of a FIR filter (3) to the output of an A/D converter (1). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of AAPA with Tomimoto with the motivation to stabilize the reading of a signal and prevent interference between the filter 108 of AAPA and the PLL circuit (106, 107, 111, 112, 113) of AAPA.

Regarding claim 10, AAPA discloses that the recording medium is an optical disc medium (Specification, Page 1, line 11).

Regarding claim 11, AAPA discloses that the recording medium is a magnetic disc medium (Specification, Page 1, lines 11-12).

Regarding claim 12, AAPA discloses that the recording medium is a semiconductor memory (Specification, Page 1, lines 12-13).

Regarding claim 20, see the rejection of claim 10.

Regarding claim 21, see the rejection of claim 11.

Regarding claim 22, see the rejection of claim 12.

7. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Tomimoto further in view of Jones (U.S. Pat. No. 6,310,909 B1).

Regarding claim 4, AAPA discloses that the filter circuit (103) is a low-pass filter, but does not explicitly disclose that it is constituted by an order equal to or lower than third order. However, Jones discloses the use of a 3rd order LPF with a converter (Col. 6, lines 12-17). It would have been obvious to one of ordinary skill in the art at the time the invention was made to

combine the teachings of AAPA in view of Tomimoto with Jones with the motivation to remove undesirable high frequency components.

8. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA in view of Tomimoto further in view of Muramatsu (U.S. Pat. No. 6,381,203 B1).

Regarding claim 9, AAPA in view of Tomimoto does not explicitly disclose an adjustment circuit for calculating a jitter value on the basis of an output of the waveform equalizer, which output is corrected by the baseline control circuit, and automatically adjusting the degree of amplification of the waveform equalizer on the basis of the calculated jitter value. However, Muramatsu discloses (Fig. 1) an adjustment circuit (70) for calculating a jitter value on the basis of an output of the waveform equalizer (jitter detection 68 takes input from waveform equalizer 66), which output is corrected by the baseline control circuit (80), and automatically adjusting the degree of amplification of the waveform equalizer on the basis of the calculated jitter value (Col. 7, lines 1-33).

Response to Arguments

9. Applicant's arguments filed July 1, 2009 have been fully considered but they are not persuasive.

(a) In response to applicant's arguments on Page 7 that AAPA fails to teach or suggest that a baseline control is performed on the output of the waveform equalizer, applicant's attention is directed to AAPA Figure 5 in which the output of the waveform equalizer (DEQ 106) is sent to a baseline controller (BaseLine 107), and further, the

output of 106 is added to (i.e. controlled by) the output of 107, and thus baseline control is performed on the output of the waveform equalizer.

(b) In response to applicant's argument on Page 7 that Tomimoto, Jones and Maramatsu all fail to disclose the feature that waveform equalization with higher accuracy is carried out by performing data optimization in the time axis direction and the amplitude direction separately in different systems, this feature on which applicant relies is not recited in the rejected claims. Although the claims are interpreted in light of the specification, limitations from the specification are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

(c) In response to applicant's argument on Pages 7 and 8 that AAPA, Tomimoto, Jones and Maramatsu all fail to disclose that the resulting readout performance is thus enhanced by separately performing baseline control on the respective outputs of the waveform equalizer and the A/D converter, applicant's attention is directed to item (a) which shows that AAPA discloses that baseline control is performed on the output of the waveform equalizer. Applicant's attention is further directed to applicant's remarks on Page 7, lines 16-17 which shows that AAPA also discloses that baseline control is performed on the output of the A/D converter.

Conclusion

10. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Mark Fischer whose telephone number is (571) 270-3549. The examiner can normally be reached on Monday-Friday from 9:00AM to 6:30PM EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hoa Nguyen can be reached on (571) 272-7579. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only.

For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Mark Fischer/
Examiner, Art Unit 2627
10/7/2009

/Peter Vincent Agustin/
Primary Examiner, Art Unit 2627